2017 DASC Report

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Introduction to the DASC

- One of the oldest sponsor groups
  - founded in 1987 as the Design Automation Standards Subcommittee
- Sponsors standards in the Electronic Design Automation Area
  - SW fo Electronics Design
- 21 companies in the Electronics industry represented
- Meets one a month, once per year Face to Face
  - Attendance runs close to 90%

2017 Highlights

- 1801.2 standard (UVM) passed
  - Used in verifying close to 70% of electronic System on Chip designs
- 1076.1 standard (VHDL AMS) passed
  - Original hardware description language (HDL)for Digital-Analog designs
- 1800 standard (SystemVerilog) on RevCom agenda for December
  - Now arguably the HDL of choice world wide

2017 Lowlights

- P1076 (VHDL) required one year PAR extension
  - One of the few individual-based WGs
  - No funding from entities as with mre DASC WGs
  - Technical writing is done on a shoestring
  - Should be finished in Q1 2018

DASC and Other Standards Groups

- Continued cooperation with Accellera and growing cooperation with Si2
  - 10 year ”Get IEEE” contract in place to allow free downloads of DASC standards
- Ongoing cooperation with JEITA
  - JEITA reps have joined DASC F2F meetings at DVCon for several years
  - DASC-JEITA joint meeting in Japan in November is now ongoing for 10 years
  - Looking forward to renewal of P2416 (LSI-Package-Board) PAR

Current Published DASC Standards

IEEE Standard #	Approved	IEC Dual Logo
1076 VHDL	2008	D
1076.1 (VHDL AMS)	2017	D
1481 (OLA)	2009	D
1492 (SDF)	2010	D
1647 (e language)	2016	
1666 (SystemC)	2011	D
1666.1 (SystemC AMS)	2016	T
1685 (IP-XACT)	2014	D
1734 (Quality IP)	2011	D
1735 (IP Encryption)	2015	
1800 (SystemVerilog)	2017 (tentative)	D
1800.2 (UVM)	2017	D
1801 (UPF)	2015	D
1850 (PSL)	2010	D
2401 (LSI Package Board)	2015	D

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D = dual logo
T = Will be proposed as Dual Standard

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DASC Standards in Development

IEEE PAR #	PAR Approved	Ballot Expected
P2415 (UHA)	2014	2018
P2416 (System Level power Modeling)	2014	2018

* PAR extension
^ in second Ballot

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DASC Standards Being Revised

IEEE PAR #	PAR Approved	Ballot Expected
P1076 (VHDL)	2017 (tentative)	2018
P1647 (e)	2017 (tentative)	2020
P1801 (UPF)	2016	2017 (in resolution)

* PAR extension
^ in second Ballot