

DASC Steering Committee Meeting

21 June 2001

Hilton Conference Center, Las Vegas

Present

Peter Ashenden <peter@ashenden.com.au>, Chair

John Willis <jwillis@ftlsys.com>, Minutes

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Agenda

1. ALF PAR (Wolfgang Roethig)
2. IEEE Standards e-Balloting (Stephen Kahofer)
3. LIB IEEE PAR (Peter Ashenden)
4. 1497 (SDF) Chair Nominations
5. CHDStd Study Group (Don Cottrell)
6. Status Reports
7. Any Other Business

1. ALF PAR (Wolfgang Roethig)

PAR Presentation

Project Title: A Standard for an Advanced Library Format (ALF) Describing Integrated Circuit (IC) technology, Cells and Blocks

Pertinent Information: New standard, 5 year cycle, expect May 2002 ballot and May 2003 completion.

Scope: ALF shall serve as the data specification language of library elements for design applications used to implement integrated circuits. The range of abstraction shall include from the RTL to the tape-out level. The language shall model behavior, timing, power, signal integrity, physical abstraction and physical implementation of library elements.

Purpose: The purpose of ALF is to provide a modeling language and semantics for functional, physical and electrical performance description of technology specific library for cell-based and block-based design. Without a standard, design implementation tools would use multiple proprietary and tool-specific library descriptions. The semantics would be defined by tool implementations only, which are subject to change and prone to mis-interpretations. Also there would be redundancy using multiple descriptions for similar library aspects. Therefore a standard is proposed to create a consistent library view suitable as a reference for all design implementation applications.

There was a long discussion concerning what the output phase should be called. As a result, “tape-out level” was changed to “physical level.” Maq was concerned that the scope was too broad.

Standards with similar scope: 1481 (PI) and (DCL).

A draft PAR has been prepared and sent to Paul Menchini. 11 voting members were present, representing a quorum. 11 in favour, none against, PAR approved by steering committee.

See documents: par4alf.5.html, alf4dasc21jun2001.ppt

2. IEEE Standards E-Balloting (Stephen Kahofer)

Summary of current activity, the E-balloting process, Corporate balloting, Benefits of E-balloting and next steps. 230+ ballots /year, 100+ invitations per year, from paper to electronic, 100 successful e-ballots. Signup: <http://standards.iee.org.db.balloting/ballotform.html>. Join IEEE-SA: <http://standards.ieee.org/sa-mem/individuals.html>. Select pool by committee. Invitation links to a sign-up URL with a hot-link to membership. Submitting to the URL results in a confirmation within 72 hours. This results in a list of eligible and ineligible balloters and balance report. Sponsor forms ballot group. E-mail balloting process: email ballot includes URL, ballot site, comment site, and 2nd notice/summary. Corporate balloting: individual, corporate (entity) and mixed. Benefits of e-balloting: shorten time by 50 days, cost-reduction (450\$ draft = 100K+\$ annually). Administrative interface: productivity and reliability. IEEE hopes to move to an all-electronic process.

3. Lib IEEE PAR (Peter Ashenden)

Peter is reviving the Lib IEEE PAR. PAR is proposed for DASC Steering Committee consideration. It addresses what goes into library IEEE and header boilerplate. It avoids the issue of distribution rights for standard source code by not addressing this issue.

Scope: The standard will specify a process for determining which items are permitted to reside in the predefined library named std defined in IEEE Standard 1076 and the library named iee defined in the associated standards. It will specify requirements on the internal documentation in the source code for such items.

Purpose: Users expect that only IEEE-approved items should reside in library IEEE, but some vendors have placed non-standard items for their tools. This standard will prevent the portability and compatibility problems that arise.

The motion to forward this PAR application to IEEE passed 10/0 with one abstention.

See documents: libieee-status-dac-2001-06-21.ppt

4. 1497 (SDF) Chair Nominations:

No one was present who could speak to this. John proposed that Brien Anderson be approved conditional on his actually being willing to do this. The motion passed 11/0.

5. CHD Std (Don Cottrell for Steve Grout)

Informative Presentation:

Provides an open standard for IC design data access. Supports customer requires for: integrated systems rather than flows, choice of design tools and provider, effective transfer of technology and effective data transfer. Sponsored by Sematech, built on top of IBM IDM API. Established as IEEE/IEC standard. Group is open as a study group. The base API was published. Provides a Reference Database and Development Kit. Levelizes the playing field by breaking down adoption barriers and providing a set of self-test compliance suites. Sematech is no longer the sponsor. Founded by industry community and SI2. Based on Cadence API. 11 Coalition companies, name changed to OpenAccess. Version 1.0 of the API on eda.org, Version 2.0 in development. Source release on V2 anticipated in 2002. Community open to any company when Version 2.0 source code is released. Don proposed to extend as an OpenAccess study group with a PAR anticipated in 2003.

A motion was to continue as a study group under "OpenAccess". The pass with two absentions.

6. Status Reports

P1076 VHDL: Latest version in circulation

ISAC: Meeting tomorrow over dinner

VHDL-PLI: no report

P1076.1 (VHDL-AMS): LRM Errata sheet, standard package proposal, mixed netlists, VHDL-AMS tool implementation status and VHDL 200x

P1076.2 (Math): Stable, may be due for rebalot (**Peter will check**)

P1076.3 (Synthesis): Group is reorganizing; Alex wanted to have proposals for a synthesizable floating point package. IEC version was approved. Would like to unify VHDL and Verilog signed/unsigned.

P1076.4 (Timing/VITAL): In process of looking at 2000 issues

P1076.6 (Synthesis Interoperability): Meeting monthly, working to extend to VHDL-93.

P1164 (Std Logic): Meeting tomorrow, address easy issues first, ballot as quickly as possible. (See document: P1164-status-dac-2001-06-21.ppt)

P1577 (OO VHDL): Quiescent, Alex asked for a copy of the PAR

Lib IEEE: Meeting tomorrow

VHDL RF/MW: Meeting tomorrow

P1364: Verilog Working Group: Tying up loose ends

P1364.1 Verilog Synthesis Subset Working Group: No report

P1481: Circuit Delay and Power Calculation Working Group: Strong ongoing work, meeting weekly

P1499: OMF: Gabe was having trouble locating the chair, any leads would be appreciated

P1497 SDF: Transferred to Brien

P1551 VHDL System and Interface based Design Working Group (VHDL+): Quiescent

P1029 Waveform and vector exchange working group: No report

Chip hierarchical design system technical data study group: Earlier

Electronic design process subcommittee: No report

ALF: Earlier

Peter will wake up chairs needing to rebalot.

Motion was made and seconded to congratulation Maq for his work.

John Hillawi reported on IEC activity; SDF needed additional experts. Verilog, second ballot was voted negative.

7. Any Other Business

John Willis insure that minutes are circulated to DASC + SC.

Peter will organize DASC column in IEEE D&TC magazine.