IEEE/IEC Dual Logo Agreement

DASC-SC Meeting

San Diego, CA

11 June 2004

IEEE

Purpose of IEEE/IEC Dual-Logo Agreement

- Avoid duplication of efforts
- Recognition of contribution
- Intellectual Property rights
- Develop maintenance procedures

IEEE

Highlights

- Approved IEEE Standards are eligible for submission
- Documents Submitted to the IEC Standardization Management Board (SMB) for consideration
- The appropriate IEC TC reviews the document (FDIS ballot). No revisions can be made.
- Both organizations agree on the designation
- Process takes about six months

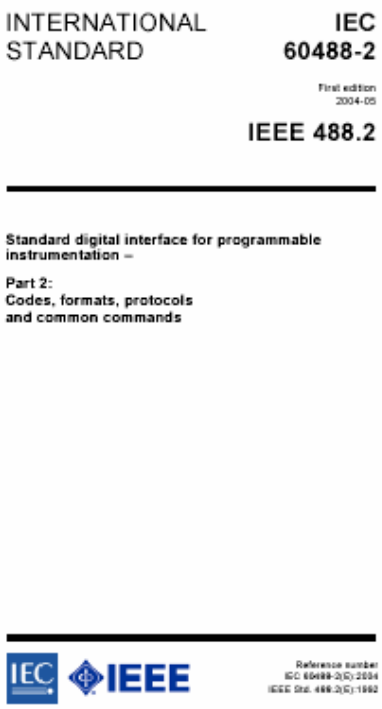
IEEE

Identifying Dual Logo Candidates

- **Candidates may be suggested by an IEEE Sponsor Chair, IEEE Working Group Chair, IEC Technical Committee or the IEC Central Office.**
- **Appropriate Parties are contacted**
  - **IEEE Working Group Chair**
  - **IEEE Sponsor Chair**
  - **US TAG (if one exists)**
  - **Chair/Secretary of relevant IEC TC**

IEEE

Example of a Dual-Logo Standard



INTERNATIONAL STANDARD

IEC 60488-2

First edition 2004-05

IEEE 488.2

Standard digital interface for programmable instrumentation –

Part 2:
Codes, formats, protocols and common commands

IEC IEEE

Reference number
IEC 60488-2(E):2004
IEEE Std. 488.2(E):1992

IEEE

Additional processes

- Revision/Maintenance Procedures developed and approved by IEC and IEEE

- Reaffirmation/Reconfirmation procedures under development

Why do this?

- Sends a strong and clear message to industry that the major technical standards developing organizations aim to cooperate toward one standard in the world wherever possible
- From a market and trade perspective, symbolizes a loosening of real and perceived barriers.

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Approved IEC/IEEE Dual Logo Standards

- IEEE Std 1076™-2002, IEEE Standard VHDL Language Reference Manual
- IEEE Std 1076.4™-2000, IEEE Standard VITAL ASIC (Application Specific Integrated Circuit) Modeling Specification
- IEEE Std 1364™-2001, IEEE Standard Verilog Hardware Description Language
- IEEE Std 1497™-2001, IEEE Standard for Standard Delay Format (SDF) for the Electronic Design Process

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Future Submissions (Confirmed)

- **IEEE Std 1232™-2002, IEEE Standard for Artificial Intelligence Exchange and Service Tie to All Test Environments (AI- ESTATE)**
- **IEEE Std 1603™-2003, IEEE Standard for an Advanced Library Format (ALF) Describing Integrated Circuit (IC) Technology, Cells, and Blocks**

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Potential Submissions

- **IEEE Std 1076.1™-1999, IEEE Standard VHDL Analog and Mixed-Signal Extensions**
- **IEEE Std 1076.6™-2004, Standard for VHDL Register Transfer Level (RTL) Synthesis**
- **IEEE Std 1364.1™-2002, IEEE Standard for Verilog Register Transfer Level Synthesis**

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