IEEE P1800 Status Report September 2004

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Membership

- Over 50 members on ieee1800 reflector
- 11 active members (F2F meetings):
  - Intel, IBM, Sun, Mentor, Cadence, Synopsys, Accellera, Verisity, Sunburst Design, Infineon, BlueSpec
  - Guests from several other companies
  - Monthly F2F meetings and good collaboration between group members

Brief Status Update

- P1800 PAR was approved in June
  - Co-sponsored by DASC-SC and CAG
- Established a P1800 work group
  - Johny Srouji as chair; Dennis Brophy as secretary
  - Had 3 F2F meetings: July, Aug, Sep
  - Reflector and web page were established
- Procedures & Policies were prepared, reviewed and approved
  - Ratified by sponsors

Brief Status Update (*cont)*

- Funded services for P1800
  - Edward Rashba prepared a valuable proposal and presented to the group
  - A small task force was formed to explore and negotiate contract terms and deliverables
  - Revised contract was reviewed by P1800 and unanimously approved
  - It was decided to appoint Oz Levia (Synopsys DR) and Victor Berman (Cadence DR) as monitors to oversee the IEEE progress

Brief Status Update (*cont)*

- Funding Resources:
  - P1800 asked Accellera to fund 50% of the IEEE funded services program cost ($120K)
    - Request was approved by Accellera board
  - Rest of the cost will be covered through participation fees:
    - Based on company revenues (above $10M)
- Errata:
  - It was agreed that all SV Errata must be submitted by 9/13 to be considered for first draft

Schedule

DATE	Mile Stone	Comment
9/13/2004	Collection of Errata	submitted Errata after this date, will be captured in the Data Base but will not included in first draft
13-Sep-04	Formation of Balloting Pool	
1-Oct-04	IEEE Contract Closure	
1-Oct-04	Initial Draft Std.	SV3.1a in IEEE style
1-Feb-05	2nd Draft Complete	Includes resolved Errata
15-Feb-05	Invitation to Ballot	
15-Mar-05	Closing on vote	
30-Mar-05	Formation of the Balloting Review Committee	
1-May-05	Ballot Resolution	
1-Jun-05	Complete Ballotable Draft	
2-Jun-05	Recirculation (as required)	
13-Jun-05	Close of Ballot	
30-Jul-05	Resolve Ballot Cmts, mod std, RevCom	Deadline is August 12. Next deadline is Oct 18
22-Sep-05	IEEE Standards Board Approval	Next deadline is Dec 6-7
15-Oct-05	Standard Publication	

SystemVerilog Errata Sub-Group

- A SystemVerilog Errata sub-group was formed:
  - To collect SV Errata and Propose solutions
  - After nomination and election process, Karen Pieper was elected to chair this sub-group
  - Accellera technical committees were moved under this sub-group
    - Kept their focus on modeling, enhancements (test-bench), assertions and DPI
    - New chairs/co-chairs for some committees
  - Focus is on Errata issues

1364 & 1800 Work Alignment

- Short Term: P1800 and P1364 project needs must be addressed:
  - P1800 – IEEE standard per our schedule
  - P1364 – Resolve Errata and continue operation of ETF and PTF. BTF to address omissions, simple extensions and encryption
- Long Term: Align languages into one LRM
  - A task force led by Victor Berman was formed to report on BTF and PTF work and propose alignment plans on SV data types

Summary

- P1800 has defined and committed to an aggressive timeline for delivering the first IEEE SystemVerilog standard
- Work group operation and progress is on track
- Structure of the group is being worked on:
  - Meeting short term needs. Keeping long term in mind
  - To enable alignment between 1364 and 1800
  - To quickly deliver a quality IEEE LRM
  - Will involve language champions
- It is doable!