

IEEE P1800  
Status Report  
November 2004

*Johnny Srouji*

The SystemVerilog logo, featuring the text "SystemVerilog" in a blue serif font. The text is partially enclosed by a green and yellow swoosh that curves around the bottom and right sides of the word.

SystemVerilog

# Brief Status Update

- Contract with IEEE Funded Services was finalized and signed
  - Noelle Humenick was assigned as the WG project manager
  - Cost is about \$130K
  - Accellera agreed to fund ~50% of the cost
  - The rest would come from member fees and Accellera would act as agent to collect them
- Bids for P1800 Technical Editor were started
  - Expect to finalize an agreement by end of this week

## Brief Status Update (*cont*)

- Errata:
  - A process for efficient P1800 ratification of Errata was presented and approved (details under: <http://www.eda.org/sv-ieee1800/Meetings/2004/October/Errata-Resolution-ProcessProposal.pdf>)
  - SystemVerilog Database Operating Procedures as well as the role of Champions was presented and approved (details under: <http://www.eda.org/sv-ieee1800/Meetings/2004/October/SystemVerilogDatabaseOperatingProcedures.pdf>)
  - Recent Errata that was approved by SV sub-WG (~40) was voted on by P1800 WG and approved

## Brief Status Update (*cont*)

- 1364 Verilog Alignment:
  - It was decided to have both 1364 and 1800 project ballots at the same time. This is to sync on dependencies between IEEE P1800 LRM and 1364
  - It was decided that 1364 sub-WG will be kept moving as is except for PTF, which will be merged into SV-CC
    - Charles Dawson, PTF chair, was elected to lead this technical committee
  - It was decided that March 2005 would be the work completion cutoff date, such that we can meet the DAC completion milestone

## Brief Status Update (*cont*)

- 1364 Verilog Alignment:
  - It was decided to move “Data Types” work, that was done in 1364 BTF, under SV-BC
    - Kathy McKinley of Cadence (leader of Data Types work) formed a task force
  - It was decided to expand the Champions role to include both P1800 and P1364
- Proposed P1800 WG structure was approved by WG
  - Officers’ election process was completed
    - Pending approval of sponsors: DASC-SC and CAG
  - Election process for 1364 SUB-WG chair was started and will close on November 21

# IEEE P1800 Structure

IEEE P1800  
SystemVerilog WG

Chair - Johny Srouji

Vice chair – Shrenik Mehta

Secretary - Dennis Brophy

Program Mgr: Noelle Humenick

LRM - TBD

Errata Chair: Karen Pieper

Chair: TBD

P1800 Errata  
Sub-WG

1364 Verilog  
Sub-WG

Champions

SV-  
BC

SV-  
EC

SV-  
AC

SV-CC &  
PTF

BTF

Encryption

Errata

(transfer/merge)

# High Level Schedule

- Nov'18: P1800 Draft2.0 completed (IEEE style; ratified Errata incorporation)
- Dec'09: TCC's close on Errata and Champions approval
- Dec'15: WG ratifies approved Errata; pass to Technical Editor
- Jan'20: P1800 Draft3.0 completed incorporating all ratified Errata
- Feb'17: P1800 Draft4.0 completed incorporating all recent recommendations; modification; and Errata
- Feb'18-Apr'11: Ballot; Results Collection; Resolution
- Apr'25: P1800 Draft5.0 completed
- May'15: ballot resolution committee approves draft; results sent to WG chair / sponsor / program manager
- Aug'12: RevCom submission deadline
- Sep'21: RevCom approves P1800
- Sep'22: Standards Board approves P1800