IEEE P1800 Status Report

ACCELLERA Board

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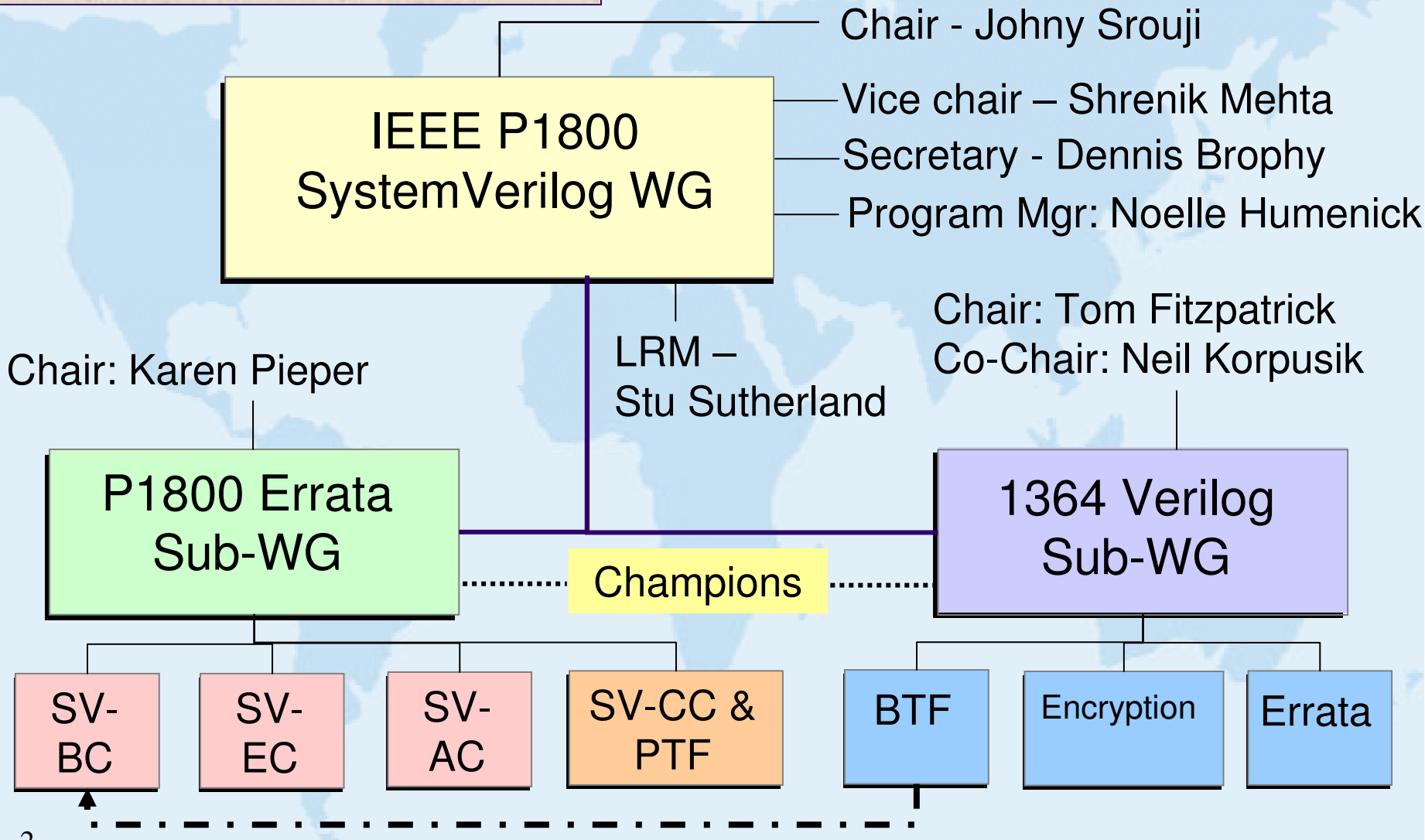
IEEE P1800 Structure



March, 2005

Major "Past" Milestones

Milestone	Due Date	Status
SystemVerilog Draft 2.0 made ready incorporating all resolved issues (upto October'04)	November 18, 2004	DONE
SystemVerilog Issues List resolve, review and approved	December 17, 2004	DONE
Verilog P1364-D5 to include: Encryption Proposal All issues approved at 12/17 P1800 meting PLI deprecation	January 13, 2005	DONE
SystemVerilog Draft 3.0 made ready - incorporating all resolved issues	January 14, 2005	DONE
SystemVerilog BALLOT Draft made ready	February 18, 2005	ON TRACK
Verilog BALLOT Draft made ready	February 18, 2005	ON TRACK

Ballot Status

- Ballot Drafts were made ready
- Ballot invitations were sent for P1800 and P1364
  - P1800 Ballot Status - 14 entities registered
    4 Users; 6 Producers; 4 Others
  - P1364 Ballot Status – 12 entities registered
    3 Users; 5 Producers; 4 Others
- Ballot Period: 22 February – 24 March
- Issues Resolution by Technical Committees by April'11
- Ballot Resolution Approvals by WG members by April'19 (F2F meeting)

Major “Next” Milestones

Feb’18, 2005	IEEE SystemVerilog Draft4.0 available for ballot; Verilog Draft6.0 ready for ballot
Feb’22-Mar’24, 2005	30-day initial ballot of SystemVerilog Draft4.0 and Verilog Draft6.0
Apr’20, 2005	technical writer prepares SystemVerilog draft5 and Verilog draft7. Secretary prepares ballot comment matrix with dispositions for recirculation. Program manager prepares cover letter to balloters.
May’20, 2005	10-day recirculation ballot of SystemVerilog draft 5 and Verilog draft 7. Results sent to WG chair / sponsor / program manager
Aug’12, 2005	RevCom submission deadline
Sep’21, 2005	RevCom approves P1800 SystemVerilog and P1364 Verilog

Brief Summary

- P1800 and P1364 are both on track
- Work-Group is getting ready for Ballot
  - Ballot resolution processes are being defined for discussion and approval on 17 February F2F meeting
- All Work-Group members are cooperative and working together on achieving our Goals
  - Excellent and Hard work by all technical committees
  - Excellent cooperation w/ IEEE Representative - Noelle Humenick

BACKUP FOILS

Organization

- Over 50 members on ieee1800 reflector
- 11 active members from Users' and EDA entities
- Appointed Officers:
  - Chair: Johny Srouji, IBM corporation
  - Secretary: Dennis Brophy, Mentor Graphics
  - Vice-chair: Shrenik Mehta, SUN corporation

P1800 Goals - The Big Picture

- Publish and Ballot SystemVerilog LRM
  - Draft by DAC 2005
- Publish and Ballot 1364 2005 LRM
  - Errata corrections
  - Consistency
  - Draft by end of 2005
- Publish a single LRM
  - Over the next 2-3 years

Brief Status Update

- Excellent and on-track progress of the WG and all technical committees
  - *See next foil for Major milestones update*
- Working on a quality draft for Verilog and SystemVerilog while resolving lots of issues
- SystemVerilog Issues Summary:
  - 278 issues have been addressed by the committees
  - 86 remain open to be addressed in a future LRM:
    - AC: 1
    - BC: 35
    - CC: 17
    - EC: 33