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# IEEE P1800 Status Report DASC-SC

June 2005

Johny Srouji



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### **Progress**

- SystemVerilog Draft 4.0 & Verilog Draft 6.0 were made ready on time for Ballot
  - Ballot Period: 22 February 24 March
- Ballot invitations were sent for P1800 and P1364
  - P1800 Ballot Status 14 entities registered
    4 Users; 6 Producers; 4 Others
  - P1364 Ballot Status 12 entities registered
    3 Users; 5 Producers; 4 Others
- P1800 WG successfully went into Ballot process
  - See next foil for first ballot results
- P1800 WG plans to go to Ballot re-circulation on June 13



# **"First" Ballot Results**

#### SystemVerilog P1800

14 eligible entities in this ballot group.

- 11 affirmative votes
- 3 negative votes with comments
- $\rightarrow$  14 ballot return = **100**% vs. required rate of 75%
- $\rightarrow$  11 affirmative votes = **78% affirmative** vs. required rate of 75%

#### Verilog P1364

13 eligible entities in this ballot group.

- 10 affirmative votes
  - 2 negative votes with comments
- $\rightarrow$  12 ballot return = 92% vs. required rate of 75%
- $\rightarrow$  10 affirmative votes = 83% affirmative vs. required rate of 75%



### Progress

- All Technical Committees worked hard in order to review, discuss and resolve about 290 ballot issues
- Several P1800 WG meetings held to review and approve Ballot Resolution
  - Ballot issues resolution and comments were approved on June 09
- P1800 WG approved SystemVerilog Draft 5.0 and Verilog Draft 7.0 for Ballot recirculation
  - 10 day ballot recirculation period will be initiated by June 13
- Excellent progress and collaboration between all WG members
  - Outstanding work by all technical committees



## **Major "Next" Milestones**

June'13, 2005	10-day recirculation ballot of SystemVerilog draft 5 and Verilog draft 7. Results sent to WG chair / sponsor / program manager
July'11, 2005	P1800 WG meeting to review ballot recirculation results
Aug'12, 2005	RevCom submission deadline
Sep'21, 2005	RevCom approves P1800 SystemVerilog and P1364 Verilog