myProject™ -P1850 PAR Detail

Submitter Email:harrydavidfoster@gmail.com
Type of Project: Revision to IEEE Standard
PAR Request Date: 27-Oct-2007
PAR Approval Date:
PAR Expiration Date:
PAR Signature Page on File: No
Status: Unapproved PAR, Revision to an Existing IEEE Standard, Std 1850-2005
Project:
Root Project: 1850-2005

1.1 Project Number: P1850
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use
1.4 Is this project in ballot now? No

2.1 Title: IEEE Standard for Property Specification Language (PSL)
Old Title: IEEE Standard for Property Specification Language (PSL)

3.1 Working Group: Property Specification Language Working Group (C/DA/1850_WG)

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3.2 Sponsoring Society and Committee: IEEE Computer Society/Design Automation (C/DA)

Contact Information for SponsorChair
Victor Berman
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Contact Information for Standards Representative
None

4.1 Type of Ballot: Corporate

4.2 Expected Date of Submission for Initial Sponsor Ballot: 02/2009

4.3 Projected Completion Date for Submittal to RevCom: 05/2009

5.1 Approximate number of people expected to work on this project: 15

5.2 Scope: This standard defines the property specification language (PSL), which formally describes electronic system behavior. This standard specifies the syntax and semantics for PSL and also clarifies how PSL interfaces with various standard electronic system design languages.

Old Scope: This standard defines the property specification language (PSL), which formally describes electronic system behavior. This standard specifies the syntax and semantics for PSL and also clarifies how PSL interfaces with various standard electronic system design languages.

5.3 Is the completion of this standard dependent upon the completion of another standard: No

5.4 Purpose: The purpose of this standard is to provide a well-defined language for formal specification of electronic system behavior, one that is compatible with multiple electronic system design languages, including IEEEStd 1076™ (VHDL), IEEE Std 1364™ (Verilog®), IEEE P1800™ (SystemVerilog®), and IEEE P1666™ (SystemC), to facilitate a common specification and verification flow for multi-language and mixed-language designs.

The proposed project will create an updated IEEE standard based upon IEEE Std. 1850-2005. The updated standard will refine IEEE standard, addressing errata, minor technical issues, and proposed extensions specifically related to property reuse and improved simulation usability.

Old Purpose The purpose of this standard is to provide a well-defined language for formal specification of electronic system behavior, one that is compatible with multiple electronic system design languages, including IEEEStd 1076™ (VHDL), IEEE Std 1364™ (Verilog®), IEEE P1800™ (SystemVerilog®), and IEEE P1666™ (SystemC), to facilitate a common specification and verification flow for multi-language and mixed-language designs.

5.5 Need for the Project: As the complexity of Very Large Scale Integration (VLSI) has grown to the degree that the traditional approaches have limitations, and the verification costs have reached 60%-70% of the development resources, the need for advanced verification methodology, with improved levels of observability of the design behavior and controllability of the verification process has become critical. Over the last decade, a methodology based on the notion of "properties" has been identified as a powerful verification paradigm that can assure enhanced productivity, higher design quality and, ultimately, faster time to market and higher value to engineers and end-users

of electronics products. Properties, as used in this context, are concise, declarative, expressive and unambiguous specifications of desired system behavior, which are used to guide the verification process. This standardization project will provide the EDA industry with a standard language for specifying electronic system behavior using properties, also referred to as a property specification language. This language will facilitate property-based verification using both simulation and formal verification, thereby enabling a productivity boost in functional verification.

5.6 Stakeholders for the Standard: Industry companies performing electronic design and verification, EDA tool providers.

Intellectual Property

6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior
to the PAR submittal to the IEEE-SA Standards Board? Yes
If yes, state date: 09/25/2007

6.1.b. Is the Sponsor aware of any copyright permissions needed for this project? No

6.1.c. Is the Sponsor aware of possible registration activity related to this project? No

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7.1 Are there other standards or projects with a similar scope? Yes
If yes, please explain:IEEE 1800 contains property specification capabilities that are currently explicitly targeted at the SystemVerilog language. P1850 property specification language is explicitly targeted at multiple hardware description languages (VHDL, Verilog, SystemC, SystemVerilog)
and answer the following:
Sponsor Organization: IEEE-DA
Project/Standard Number: 1800
Project/Standard Date: 10/15/2005
Project/Standard Title: SystemVerilog—Unified Hardware Design, Specification, and Verification Language

7.2 Future Adoptions
Is there potential for this standard (in part or in whole) to be adopted by another national, regional, or international organization? Do not know at this time

7.3 Will this project result in any health, safety, security, or environmental guidance that affects or applies to human health or safety? No

7.4 Additional Explanatory Notes: (Item Number and Explanation)