Japan NC & JEITA/EDA-TC Update IEC/TC93/WG2

on 18-22 September 2006 in Berlin, Germany

JEITA
社団法人 電子情報技術産業協会
Japan Electronics and Information Technology Industries Association

EDA-TC/STD-TSC in JEITA
WG2 in TC93-JP
Sony
Shigemi Saito

- Outline -

- JEITA Structure and Management
- EDA-TC Current major activities
- SystemC-TG, SytemVerilog-TG Activities
- DASC-”EDA-TC” Collaboration Structure
- Outline of EDSFair 2007

JEITA : Japan Electronics and Information Technology Industries Association

(URL http://www.jeita.or.jp)

JEITA Structure and Management

JEITA Japan Electronics and Information Technology Industries Association

- **Information Systems Board**
- **Personal Informatization Board**
- **Digital Home Appliances Board**
- **Industrial Equipment and Social Systems Board**
- **Display Devices Board**
- **Electronic Components Board**
- **Semiconductor Board(JEITA-JSIA)**
  - **Semiconductor Industrial Affairs Committee**
  - **Semiconductor International Affairs Committee**
  - **Semiconductor Technology Committee**
    - Marketing Committee
    - Road Map Committee
    - **EDA Technical Committee(EDA-TC)**
      - **Chair: Y.Sugiyama(Fujitsu)** ☆
      - **Members: 19 Companies**
        Fujitsu, Matsushita, NEC EL, Oki, Toshiba, Renesas, Sanyo, Sharp, Sony, Rohm, Seiko Epson, Synopsys, DNS Cadence, JEDAT, Mentor, Ricoh, Zuken, Marubeni.Sol

◆*EDA Technical Committee was formed to handle EDIF 2.0 standard as one of technical committees in JEITA (former EIAJ) in April 1990 .*

EDA-TC Current major activities(1)

1. EDSFair Executive Committee

Chair : M.Nadaoka(Oki)

- To organize and support events to promote and encourage EDA technology and standards. To sponsor the EDS Fair exhibition show

2. Study Groups

PDS (Physical Design Standardization) Study Group

- Chair: T.Okumura(Fujitsu)☆
- Member : 13 Companies, Meeting Frequency : Monthly
  Cadence, Fujitsu, JEDAT, Matsushita, Mentor, NEC EL, Oki, Renesas, Ricoh, Sanyo, Sharp, Sony, Synopsys
- To investigate standardization for design methodologies, libraries, and their benchmarks in nanometer-era physical design

EDA-TC Current major activities(2)

3. Standardization Technical Subcommittee(STD-TSC)

- Chair : S.Saito(Sony) ☆

- Members: Experts from Academia, Semiconductor industries and EDA industries

Members: 22members from 17 Companies and 2 Universities

- To contribute EDA related standardization efforts by supporting EDA standards related groups and organizations such as Accellera, IEEE/IEEE-SA, IEEE/DASC, IEC/TC93, OSCI...

- Hosted Meeting of IEC/TC93 Design Automation on 5-9 September 2005 in Nara, Japan

■SystemC Task Group

■SystemVerilog Task Group

SystemC-TG Activities

- SystemC-TG(Oct. 2003~)
  - Member : 13 Companies
    - Chair: T.Hasegawa(Fujitsu)
    - Cadence, Fujitsu, Matsushita, Mentor, NEC EL, Oki, Renesas, Ricoh, Sanyo, Sony, Synopsys, Toshiba
  - Meeting Frequency : 10 times/year
  - Joined IEEE P1666-WG as a voting member, and Contributed to IEEE Std. 1666-2005 (Dec, 2005) :
    - Submitted over 50 Issues and Requests, and all Resolved
  - Creating SystemC Related Technical Summary Report :
    - TLM Guide, SystemC 2.1 Reference Sim.(done), Synthesis Subset

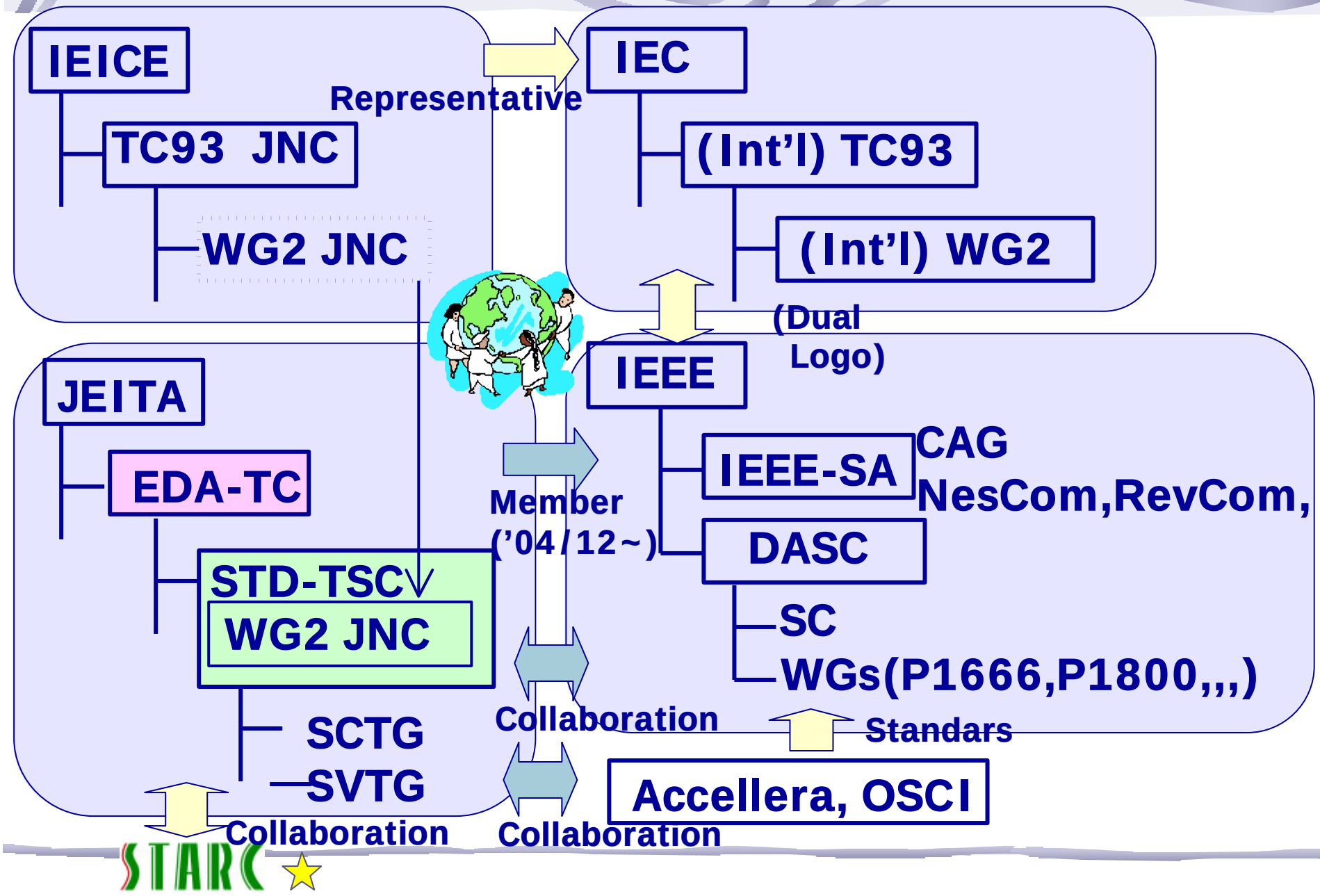
SystemVerilog-TG Activities

- SystemVerilog-TG(Oct. 2003~)
  - Member : 10 Companies
    - Chair: K.Hamaguchi(Matsushita)
    - Cadence, Fujitsu, Matsushita(2 members), Mentor, ONW, Renesas, Sanyo, Synopsys, Toshiba, Zuken
  - Meeting Frequency : 5 times/year
  - Joined IEEE P1800-WG as a voting member, and Contributed to IEEE Std. 1800-2005 (Nov, 2005) :
    - Submitted over 32 Issues and Requests, and almost Resolved
  - Creating the “Technical term dictionary” for Japanese industry standard

Collaboration of two task groups

- Collaboration of SystemC-TG and SystemVerilog-TG
  - Co-hosting the SystemC/SystemVerilog User's Forum in EDSFair in 2007 at Yokohama

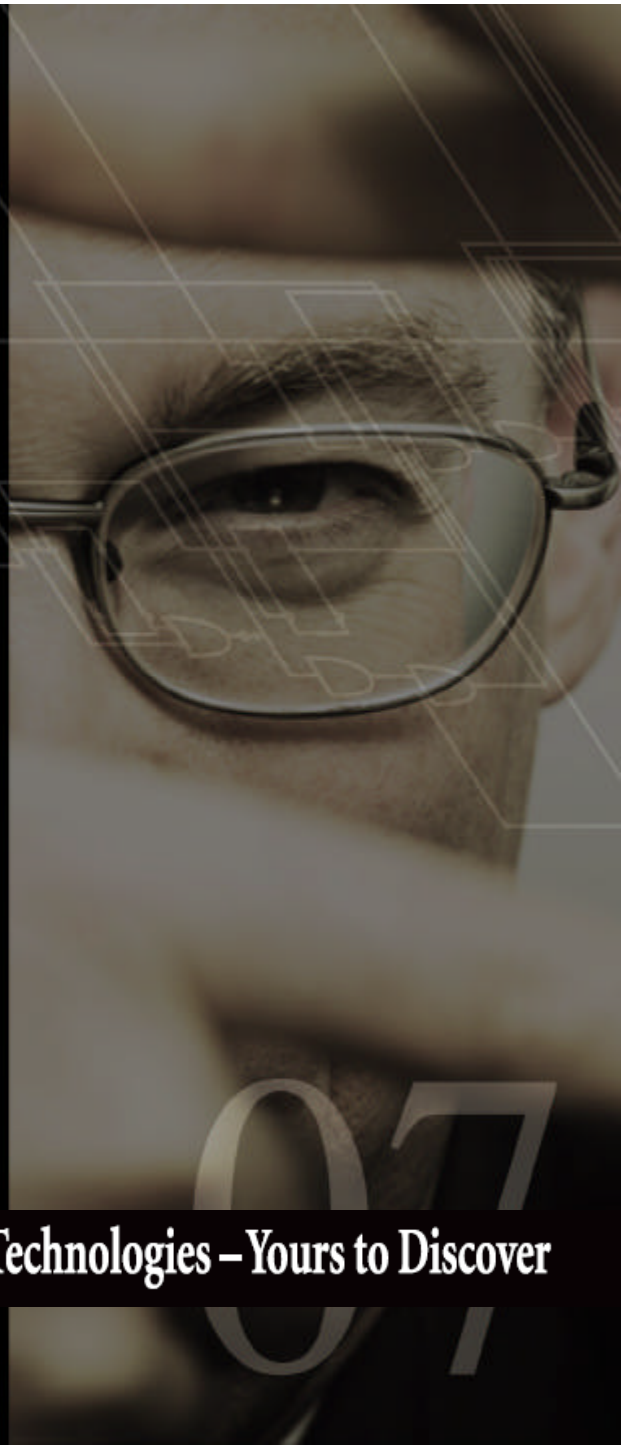
DASC-"EDA-TC" Collaboration Structure



Electronic Design and Solution Fair 2007

with FPGA/PLD Design Conference

Outline of EDSFair 2007



Electronic Design and Solution Fair 2007

Executive Committee

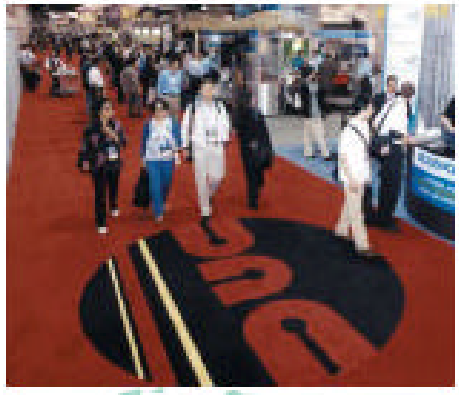
General-Chair Mitsuru Nadaoka

www.edsfair.com

What is EDSFair?

DATE

EDSFair



DAC

JEITA

EDA CONSORTIUM

■ **EDSFair is one of three major EDA exhibitions held in Japan.**

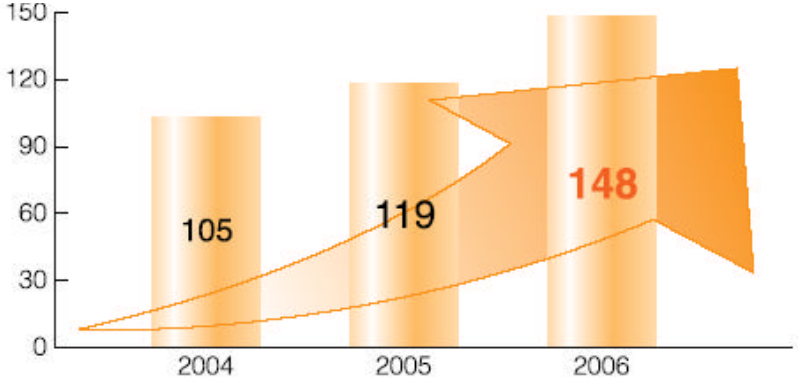
(EDAC is supporting EDSFair to attract overseas Emerging companies)

Comparison of DAC and EDSFair

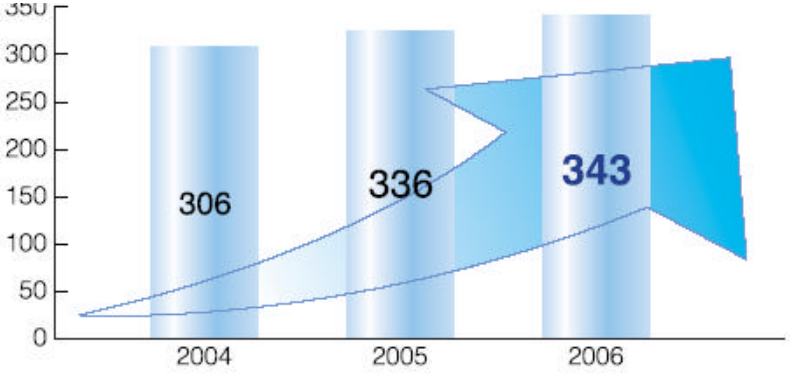
Exhibition period and visitor numbers

Name of the exhibition	Date	Location	Number of vistior
DAC (Design Automation Conference 2005)	June 13 - 17, 2005	California, U.S.A	14,700
EDSFair 2006 (Electornic Design and Solution Fair 2006)	January 26 - 27, 2006	Yokohama, Japan	11,003

■Number of Exhibitors



■Number of Booths



Outline of EDSFair 2007

View of Pacifico Yokohama

■Schedule :
January 25-26, 2007　10:00 to 18:00

■Location :
Pacifico Yokohama, JAPAN

■Constituent part :
Exhibition, Exhibitor's seminar,
FPGA/PLD Design Conference,
SystemC / SystemVerilog User Forum

■Simultaneous event
Asia and South Pacific Design Automation Conference (ASP-DAC) 2007

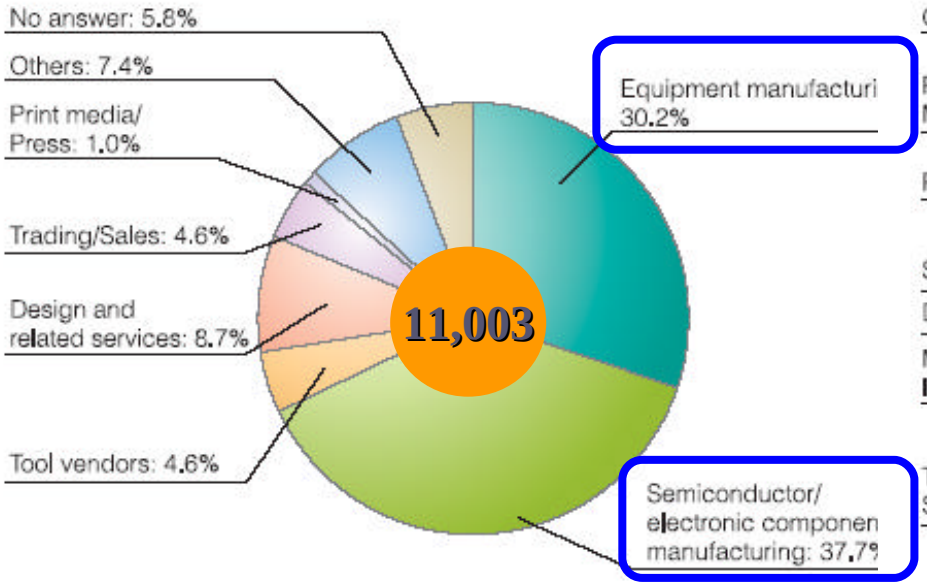
■Sponsor :
Japan Electronics and Information Technology Industries Association (JEITA)

■Cooperation :
Electronic Design Automation Consortium (EDAC)

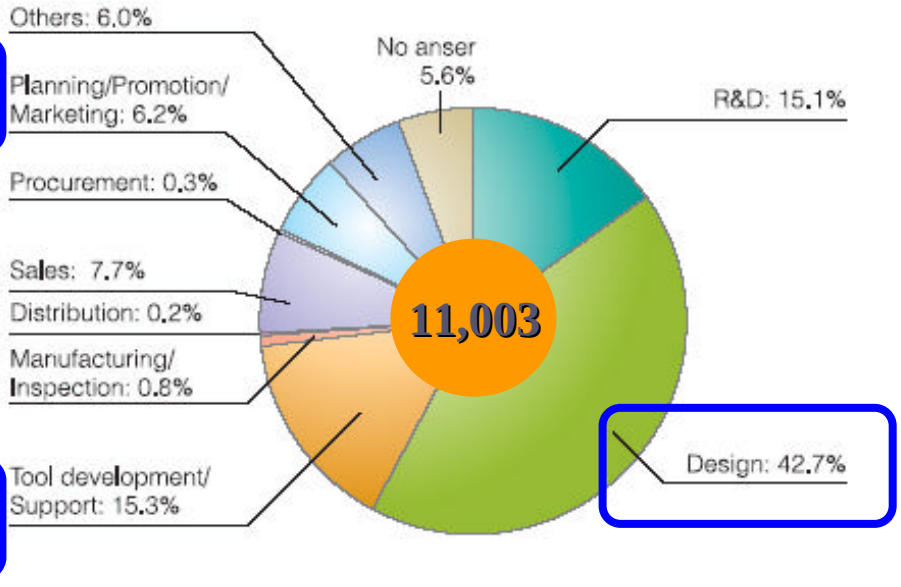
■Support :
Ministry of Economy, Trade and Industry of Japan (METI)
Embassy of United States of America in Japan

Visitor Profile

Business Category



Occupation Category



Visitors are not only Semiconductor companies but System companies

Visitors are not only EDA engineers but Designers.

Objectives of EDSFair

1. To promote and disseminate the state-of-art information of design solutions, design technologies, and EDA technologies required for the latest electronic systems or semiconductors.

2. To contribute for development of the electric device industry through above activities.

- **To achieve these objectives, we will**
  Provide Opportunities for Communications between Exhibitors and Visitors as much as possible

Features of EDSFair 2007

- Promo Word
  World-Leading Technologies - Yours to Discover

- Main Projects to achieve objectives are as follows

  - Attraction of “Emerging companies"
  by Emerging Company Area
  - Tutorials for the beginners and on Technology trend
  at Special Presentation Stage

  These are planed by visitor survey analysis result

To get more visitors
We will do Aggressive Promotion by Media
Before and After Exhibition

Appendix

Project for Emerging companies

- “Emerging Company Area”

This is special section for Emerging companies, "Low cost“ and "High added value".

This Area is just for the exhibitors, which have not exhibited no more than twice in the past EDSFair Exhibitions.

Project for Emerging companies (2)

- As Emerging Company Event
  on the Previous day of EDSFair, January 24.

We are planning "Seminar on How to establish Sales channel in Japan" **for** Emerging Companies.

- Questionnaire for Emerging Company
  To be sent in next month via EDAC.
  (Example) What are your requests for EDSFair ?

Special Presentation Stage

- Location is in the Exhibition Hall
- Program will be:

Technology Trend Presentations & Panel Discussions on

- **-Foresights of Semiconductor Industry and its Technology**
- **-ESL**
- **-DFM & Nanometer Design Challenge**
- **-Analog / RF**
- **-SiP Design Technology**

Emerging Company Area Exhibitor Presentation

(This will be Heavily announced as one of the key event for EDSFair 2007)

Aggressive Promotion by Media before Exhibition

To get more visitors

■We will ask following Japanese key media to cover EDSFair

Nikkei Electronics EDA Online, EETimes Japan, EDN Japan, EDA Express, etc.

We will submit “Special column” to these media on

Exhibit highlight, Hot topics, What’s new, How to walk EDSF, etc.

■These EDSFair topics will be delivered via E-blast by key media and EDSFair.