Agenda of IEEE DASC-JEITA EDATC meeting

- Date : 17:30 – 19:00 24th January, 2008

- Place : E202 room at Pacifico Yokohama

- Attendees : Victor Berman, Dennis Brophy,
  Steve Bailey, Stan Krolikoski,
  Saito-san, Yamada-san, Ohta-san,
  Nakamori-san, Karatsu-san, Kambe-san,
 Furui-san, Takahashi-san, Kojima

Agenda of IEEE DASC-JEITA EDATC meeting

- **Agenda**

  - Welcome and Introduction   by all

  - EDA-TC updates   by Saito-san/Kojima

  - DASC Updates   by Victor

  - Key initiatives

    - Power Format   by Steve/Yamada-san/Nakamori-san

    - System Verilog(1800) and Verilog HDL(1364)

    - System C(1666)

    - IEEE SA Tokyo meeting on 14May2008 by Dennis/Saito-san

    - Others (OVM...)   by Stan/Dennis

  - Adjourn, move to the dinner place "ARIJO"

    http://r.gnavi.co.jp/p711400/
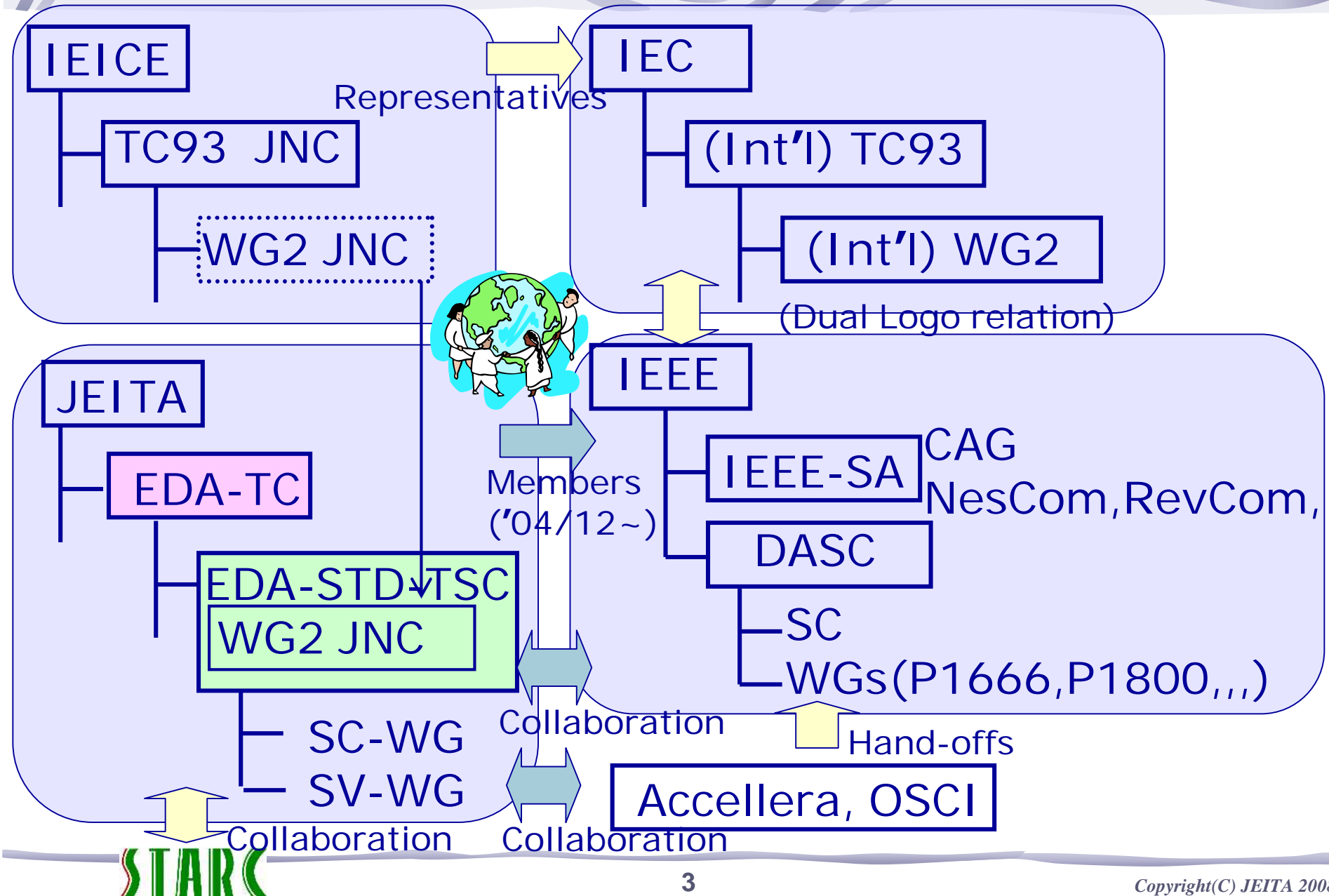
IEEE DASC – JEITA EDA-TC Annual meeting

24th September 2008 in Yokohama, Japan

JEITA

社団法人 電子情報技術産業協会
Japan Electronics and Information Technology Industries Association

JEITA EDA-TC, Special Member
TC93 WG2, Co-convener
Satoshi Kojima

- Outline -

- JEITA Structure and Management

- EDA-TC Structure

- EDA-TC Current major activities

- SystemC-WG, SytemVerilog-WG,

   Power Format Feasibility-SG activities

JEITA　 : Japan Electronics and Information Technology Industries Association
　　　　　 (URL http://www.jeita.or.jp)
EDA-TC : EDA Technical Committee
　　　　　 (URL http://eda.ics.es.osaka-u.ac.jp/jeita/eda/index.html)
EDSFair : Electronic Design and Solution Fair
　　　　　 (URL http://www.edsfair.com/e/)

JEITA Structure and Management

JEITA Japan Electronics and Information Technology Industries Association

- Information Systems Board
- Personal Informatization Board
- Digital Home Appliances Board
- Industrial Equipment and Social Systems Board
- Display Devices Board
- Electronic Components Board

Formal Member : 374
Supporting Member : 146

Semiconductor Board(JEITA-JSIA)

- Semiconductor Industrial Affairs Committee
- Semiconductor International Affairs Committee

Semiconductor Technology Committee

- Marketing Committee
- Road Map Committee

EDA Technical Committee(EDA-TC)

- Members: 19 Companies
  Fujitsu, Matsushita, NEC EL, Oki, Toshiba, Renesas, Sanyo, Sharp, Sony, Rohm, Seiko Epson, Synopsys, DNS Cadence, JEDAT, Mentor, Ricoh, Zuken, Marubeni.Sol

◆ *EDA Technical Committee was formed to handle EDIF 2.0 standard as one of technical committees in JEITA (former EIAJ) in April 1990 .*

EDA-TC Structure

EDA Technical Committee   Chair: S. Saito(SONY)

Acceleration of Standardization

EDA Standardization Technical Sub-Committee
Chair : T.Yamada (SANYO), Vice-chair : M.Ohta (Matsushita)

— SystemC Working Group
Chair : T.Hasegawa (Fujitsu)

— SystemVerilog Working Group
Chair : K.Hamaguchi (Matsushita)

— Power Format Feasibility Study Group
Chair : T.Nakamori (Fujitsu)

Proposal for Technical Problems

NPD(Nano-scale Physical Design) Working Group

Chair: T.Okumura (Fujitsu VLSI)

Promotion of EDA Technology

EDSFair 2008 Executive Committee

Chair : T.Akiyama (Renesas)

1. EDSFair Executive Committee

- Chair: T.Akiyama (Renesas)
- To organize and support events to promote and encourage
  EDA technology and standards.
- To sponsor the EDS Fair exhibition show

2. NPD (Nano-scale Physical Design) Working Group

- Chair: T.Okumura (Fujitsu VLSI)
- Meeting Frequency : Monthly
- Member : 8 Companies,
  Fujitsu, JEDAT, Matsushita, NEC EL, Renesas, Ricoh, Sanyo, Sony

- To investigate DFM technology, plan/do benchmarks related with
  parasitic extraction and delay calculation

3. EDA Standardization Technical Subcommittee (EDA STD-TSC)

- Members: Experts from
        Academia, Semiconductor industries and EDA industries
- Members: 23 members from 17 Companies and 2 Universities

- To reflect opinions on technical and business issues
  as a group of EDA power users to De Jure standard bodies
  such as IEEE-SA, IEEE-DASC & IEC/TC93.

- To raise issues on design flows to solve today and future
  design issues from member companies as an IDM and to propose
  what standard can contribute to solve as a part of solution

■ SystemC Working Group
■ SystemVerilog Working Group
■ Power Format Feasibility Study Group

Member of EDA STD-TSC (1)

Chair   : <u>Takashi Yamada</u> (SANYO Electric Co., Ltd.)

Vice-Chair   : <u>Mitsuyasu Ohta</u> (Matsushita Electric Industrial Co., Ltd.)

Member   : <u>Saito Shigemi</u> (Sony Corporation)

        (*EDA-TC Chair)

        <u>Kaoru Kawamura</u> (FUJITSU Limited.)

        <u>Toshiyasu Akiyama</u> (Renesas Technology Corporation)

        (*EDSFair Executive Committee Chair)

        <u>Yoshitada Fujinami</u> (NEC Electoronics Corporation)

        <u>Takeshi Nishimoto</u> (Sharp Corporation)

        <u>Fumihiro Minami</u> (TOSHIBA CORPORATION)

        <u>Takeshi Asai</u> (ROHM CO., LTD.)

        <u>Takashi Kumagai</u> (SEIKO EPSON CORPORATION)

        <u>Mitsuru Nadaoka</u> (OKI Electric Industry Co., Ltd.)

Member of EDA STD-TSC (2)

Special Member : <u>Satoshi Kojima</u> (NEC System Technologies. Ltd.)
          (* WG2 Co-Convener)
          <u>Takashi Aikyo</u> (STARC)
          <u>Takashi Hasegawa</u> (FUJITSU Ltd.)
           (* SystemC WG Chair)
          <u>Hiroshi Imai</u> (TOSHIBA CORPORATION)
           (* SystemC WG Vice-Chair)
          <u>Kasumi Hamaguchi</u> (Matsushita Electric Industrial Co., Ltd.)
           (* SystemVerilog WG Chair)
          <u>Takaaki Akashi</u> (Nihon Synopsys Co.,Ltd.)
           (* SystemVerilog WG Vice-Chair)
          <u>Kenji Goto</u> (Cadence Design Systems, Japan)
           (* SystemVerilog WG)
          <u>Okumura Takaaki</u> (FUJITSU VLSI Limited.)
           (* Nano-scale Physical Design WG Chair)
          <u>Tamio Hoshino</u> (Applistar Corporation)
          <u>Kumiko Ishiko</u> (FUJITSU Micro Solutions Ltd.)

Member of EDA STD-TSC (3)

Special Member (Cont'd) : Tutomu Nakamori (FUJITSU Ltd.)
                                          (* Power Format Feasibility Study WG Chair)

Guest Member : Takashi Kambe (Kinki University)
                   (*TC93 JNC Chair)
                   Masaharu Imai (Osaka University)
TC93   : Osamu Karatsu (SRI International)
                   (*TC93 Chair)
                   Yoshiharu Furui (STARC)
                   (*TC93 JNC Secretary)
Bureau   : Noboru Furukawa (JEITA (EDASTD-TSC))
                   Kogo Iwabuchi (JEITA (EDASTD-TSC))
                   Susumu Kawai (IEICE (TC93))

SystemC-WG Activities

■ SystemC Working Group (Oct. 2003~)

- Member : Top Level SystemC Experts from 12 Companies
  - Chair: T.Hasegawa(Fujitsu)
  - Cadence, Fujitsu, Matsushita, Mentor, NEC EL, Oki, Renesas, Sanyo, Sony, Synopsys, Toshiba

- Meeting : Monthly

- Past outcomes:
  - Contributed to IEEE Std. 1666-2005 (Dec, 2005) as a voting member
  - Developed the outline of the Coding Style Guideline for the High Level Synthesis with SystemC

- Current activities:
  - Prepare upcoming standardization activity of TLM and Synthesis Subset of SystemC (Review OSCI's draft documents, and submitted issue reports to OSCI)
  - Sponsor the annual Japan SystemC User's Forum 2005 thru 2007 in conjunction with the EDSF at Yokohama
  - Execute the Survey for SystemC, and share the result with other regional SystemC User Group (World-Wide)

SystemVerilog-WG Activities

- **SystemVerilog-WG** (Oct. 2003~)
  - Member : 10 Companies
    - Chair: K.Hamaguchi(Matsushita)
    - Cadence, Fujitsu, Matsushita(2 members), Mentor, ONW, Renesas, Sanyo, Synopsys, Toshiba, Zuken

  - Meeting : Bi-monthly

  - Joined IEEE P1800-WG as a voting member, and Contributed to IEEE Std. 1800-2005 (Nov. 2005) :
    - Over 32 issues/requests through reviews has almost adopted
  - Join IEEE P1800-2008 WG (Integration of Verilog and SystemVerilog) as the reviewer, and will participate in a vote
    - Submitted 35 issues in May 2007
    - Re-submitted updated issues list in Nov. 2007

Power Format Feasibility SG Activities

■ **Power Format Feasibility Study Group** (Oct. 2007~Mar.2008)

- Member : 7 Companies
  - Chair: T.Nakamori (Fujitsu)
  - Fujitsu, Matsushita, SONY, Renesas, Sanyo, Toshiba (2 members) SEIKO EPSON

- Meeting : Monthly

- Study capabilities of two formats such as UPF and CPF from a viewpoint of practical use for SoC design flow
- Complete UPF vs. CPF comparison table
  - Scope: Multi-voltage and Shut-off mechanism
  - Priority: #1=Verification and Synthesis, #2=Library, Formal and Rule Check
  - To clarify the difference of two formats
- To propose new initiatives on power format to EDA-TC